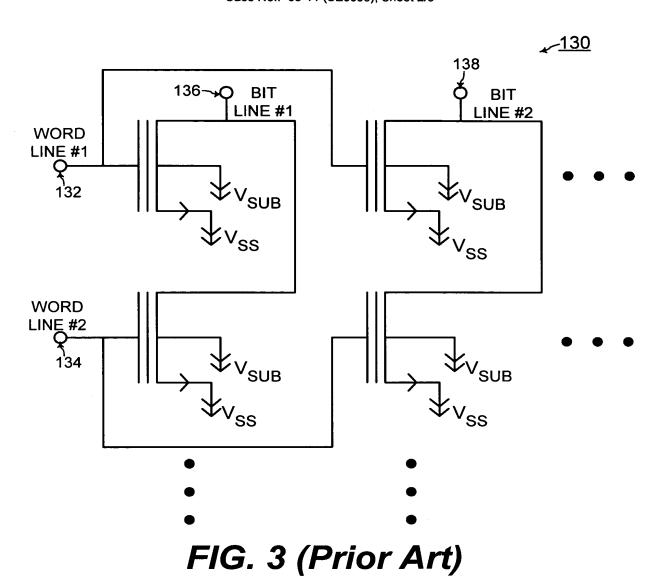


FIG. 2 (Prior Art)



A[20:16]

Address Generator 156

Sector Address
Generator

A[15:7]

Address Generator

Column Address
Generator

Generator

A[6:0]

FIG. 4 (Prior Art)

Title: Cycling through Addresses of a Memory Device with Minimized Charge Gain Failure Inventor(s): Wan Yen Teoh and Che Seong Law Case No.: 03-11 (SE0099), Sheet 3/9

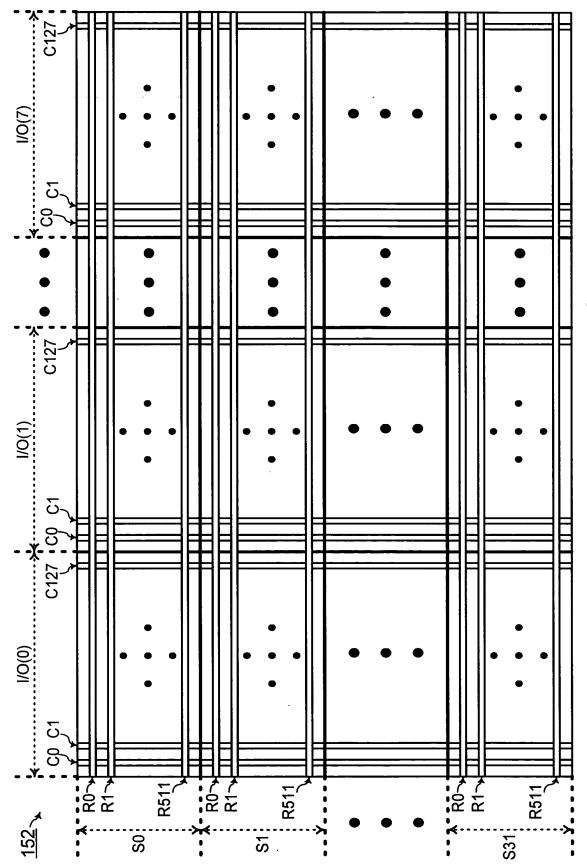
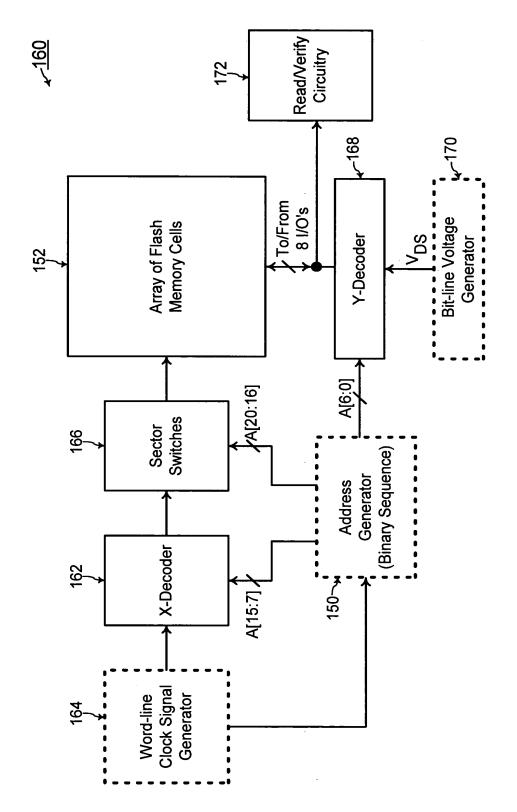


FIG. 5 (Prior Art)

Title: Cycling through Addresses of a Memory Device with Minimized Charge Gain Failure Inventor(s): Wan Yen Teoh and Che Seong Law Case No.: 03-11 (SE0099), Sheet 4/9



F/G. 6

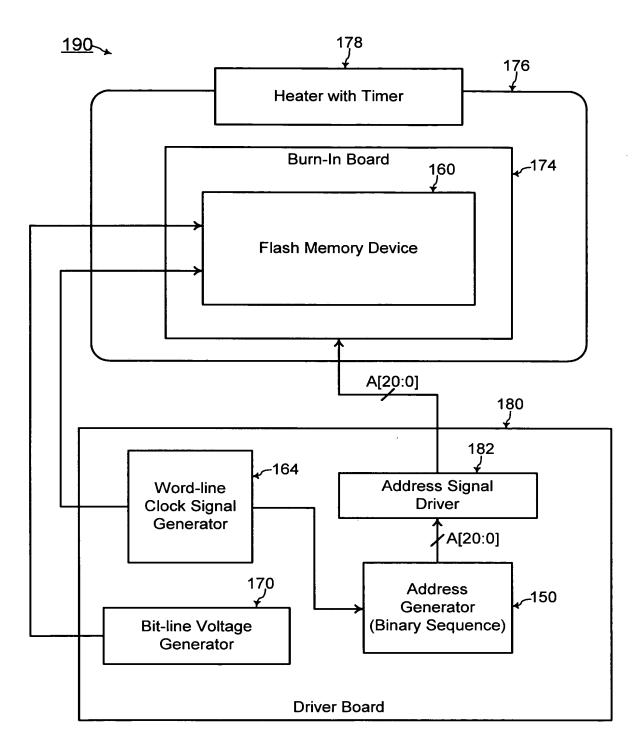
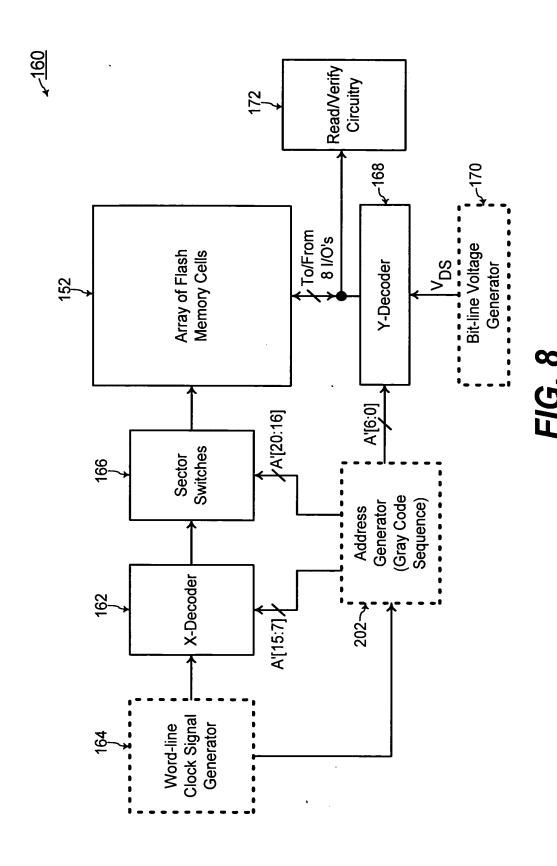


FIG. 7

Title: Cycling through Addresses of a Memory Device with Minimized Charge Gain Failure Inventor(s): Wan Yen Teoh and Che Seong Law Case No.: 03-11 (SE0099), Sheet 6/9



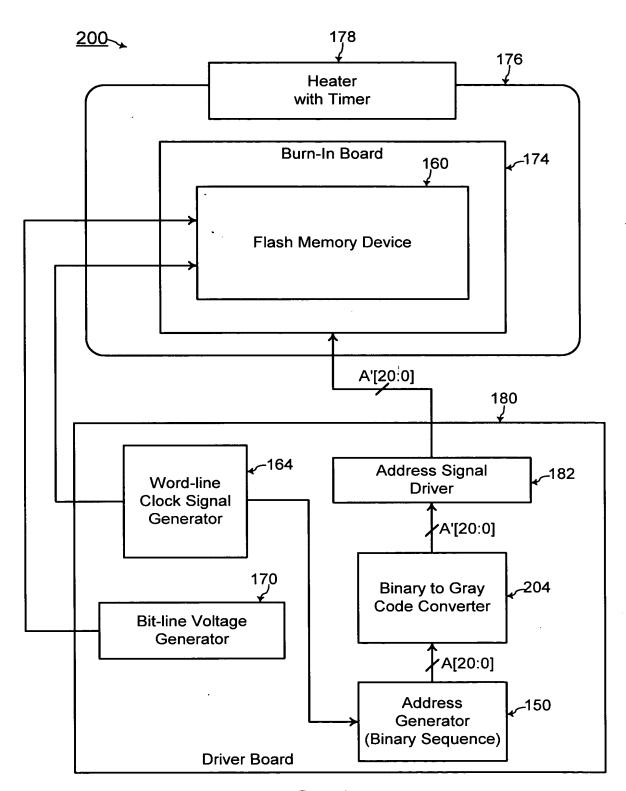
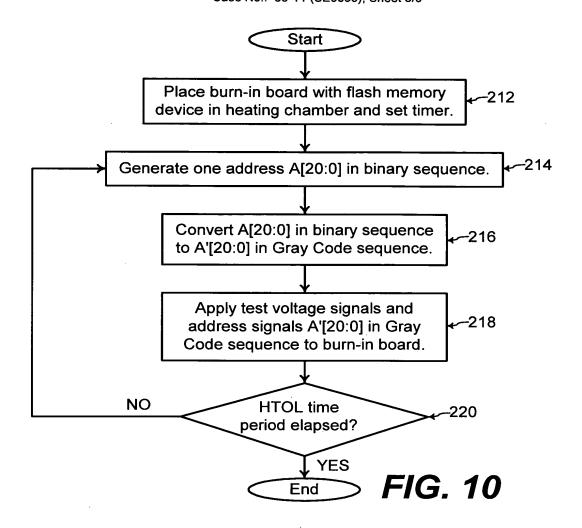


FIG. 9



302	306	304	308
Binary Sequence A2 A1 A0	# of Bit Transitions	Gray Code A'2 A'1 A'0	# of Bit Transitions
0 0 0		0 0 0	
0 0 1	1	0 0 1	1
0 1 0	2	0 1 1	1
0 1 1	1	0 1 0	1
1 0 0	3	1 1 0	1
1 0 1	1	1 1 1	1
1 1 0	2	1 0 1	1
1 1 1	1	1 0 0	1
0 0 0	3	0 0 0	1

FIG. 11

Title: Cycling through Addresses of a Memory Device with Minimized Charge Gain Failure Inventor(s): Wan Yen Teoh and Che Seong Law
Case No.: 03-11 (SE0099), Sheet 9/9

	312	314	316
	Experimental Condition	Row Location for Charge Gain Failure	Quantity Failed
322->	Ascending Binary	Row 0, Sector 0	1/90 Units (1 bit failed)
324	Descending Binary	Row 511, Sector 31	2/90 Units (1 bit failed)
326->	Descending Binary with A15 Grounded.	Row 495, Sector 31	4/90 Units (1 bit failed)
328->	Descending Binary with A14 Grounded.	Row 503, Sector 31	2/90 Units (1 bit failed)
330->	Gray Code	No Failure	No Failure

FIG. 12

